CPU AND ADDRESS/DATA BUS

UNCLASSIFIED

CF351L05-01

RISK ASSESSMENT: *Low*

SAFETY CONSIDERATIONS:

Electrical Shock Hazard

Electrostatic Discharge

ENVIRONMENTAL CONSIDERATIONS:

None

TERMINAL LEARNING OBJECTIVE

ACTION: Identify the CPU Address and Data Bus operations.

CONDITIONS: Given a classroom environment, Computer Aided Instruction (CAI) workstation, NIDA electronic trainer, and official OMEMS reference material.

STANDARDS: Correctly answer 7 of 10 questions on the CPU Address and Data Bus operations.

Enabling Learning Objective

ACTION: Explain the functions of the V30 Microprocessor pins.

CONDITIONS: Given a classroom environment, Computer Aided Instruction (CAI) workstation, NIDA electronic trainer, and official OMEMS reference material.

STANDARDS: Correctly answer 7 of 10 questions on the CPU Address and Data Bus operations.

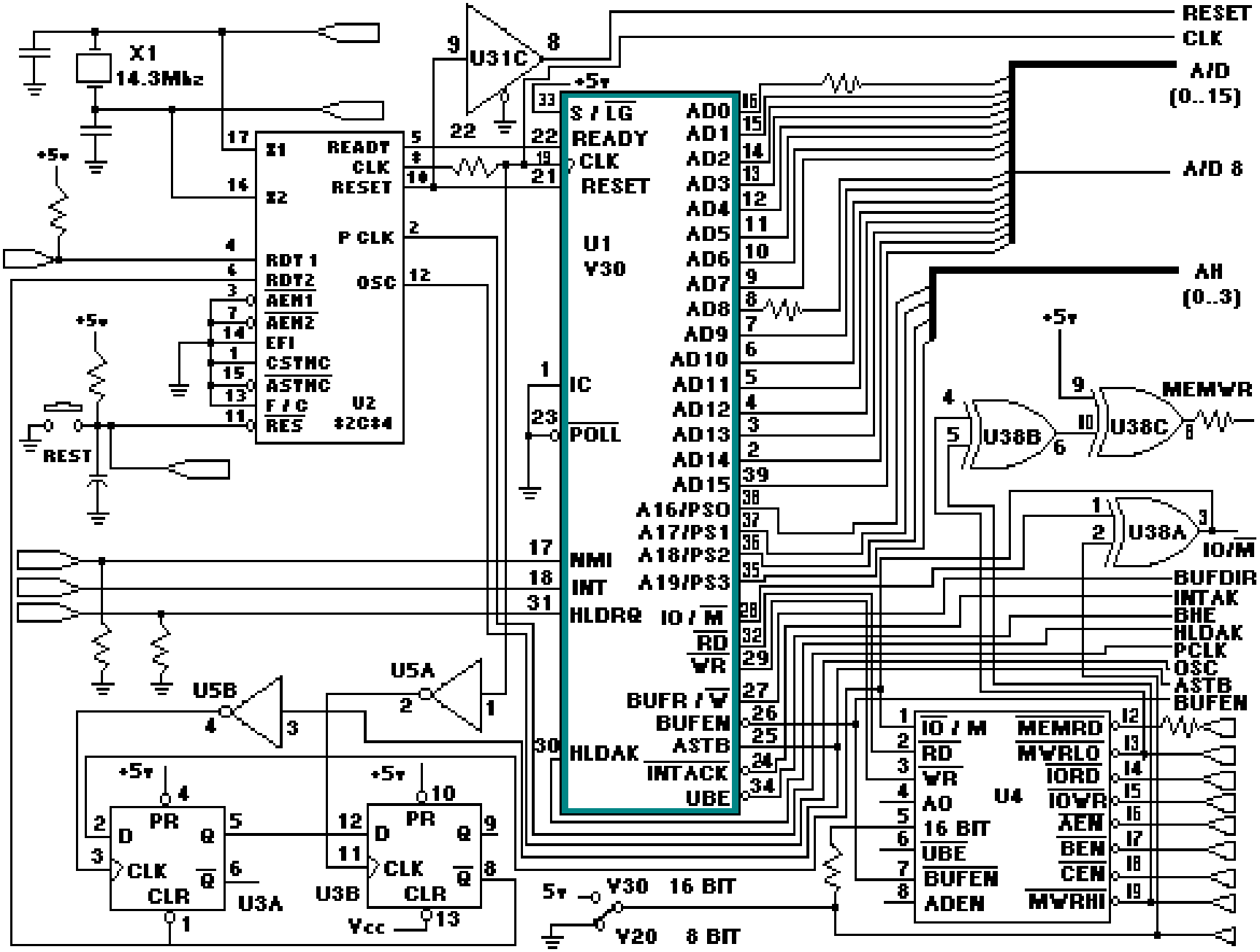
V30 U1 Microprocessor

Component designation is U1 on the schematic.

It is almost identical to the 8086 in operation except that some of the pin names have been changed.

The data bus and the ALU are both 16-bit.

It can execute both 8086 and 8080 instructions.


X1
14.3Mhz
+5v
U31C
RESET
CLK
A/D
(0..15)
A/D 8
AH
(0..3)
U1
V30
S / LG
READY
CLK
RESET
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
A16/PS0
A17/PS1
A18/PS2
A19/PS3
IO / M
RD
WR
BUFR / R
BUFEN
ASTB
INTACK
UBE
IC
POLL
NMI
INT
HLDRQ
HLDAK
U2
82C84
Z1
Z2
READY
CLK
RESET
P CLK
OSC
RDY1
RDY2
AEN1
AEN2
EFI
CSYNC
ASYNC
F / C
RES
REST
U38B
U38C
MEMWR
U38A
IO/M
BUFDIR
INTAK
BHE
HLDAK
PCLK
OSC
ASTB
BUFEN
U5A
U5B
U3A
U3B
PR
D
CLK
CLR
Q
Vcc
5v
Y30 16 BIT
Y20 8 BIT
U4
IO / M
RD
WR
A0
16 BIT
UBE
BUFEN
ADEN
MEMRD
MWRLO
IORD
IOWR
AEN
BEN
CEN
MWRHI

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Enabling Learning Objective

ACTION: Identify the Clock Generator functions.

CONDITIONS: Given a classroom environment, Computer Aided Instruction (CAI) workstation, NIDA electronic trainer, and official OMEMS reference material.

STANDARDS: Correctly answer 7 of 10 questions on the CPU Address and Data Bus operations.

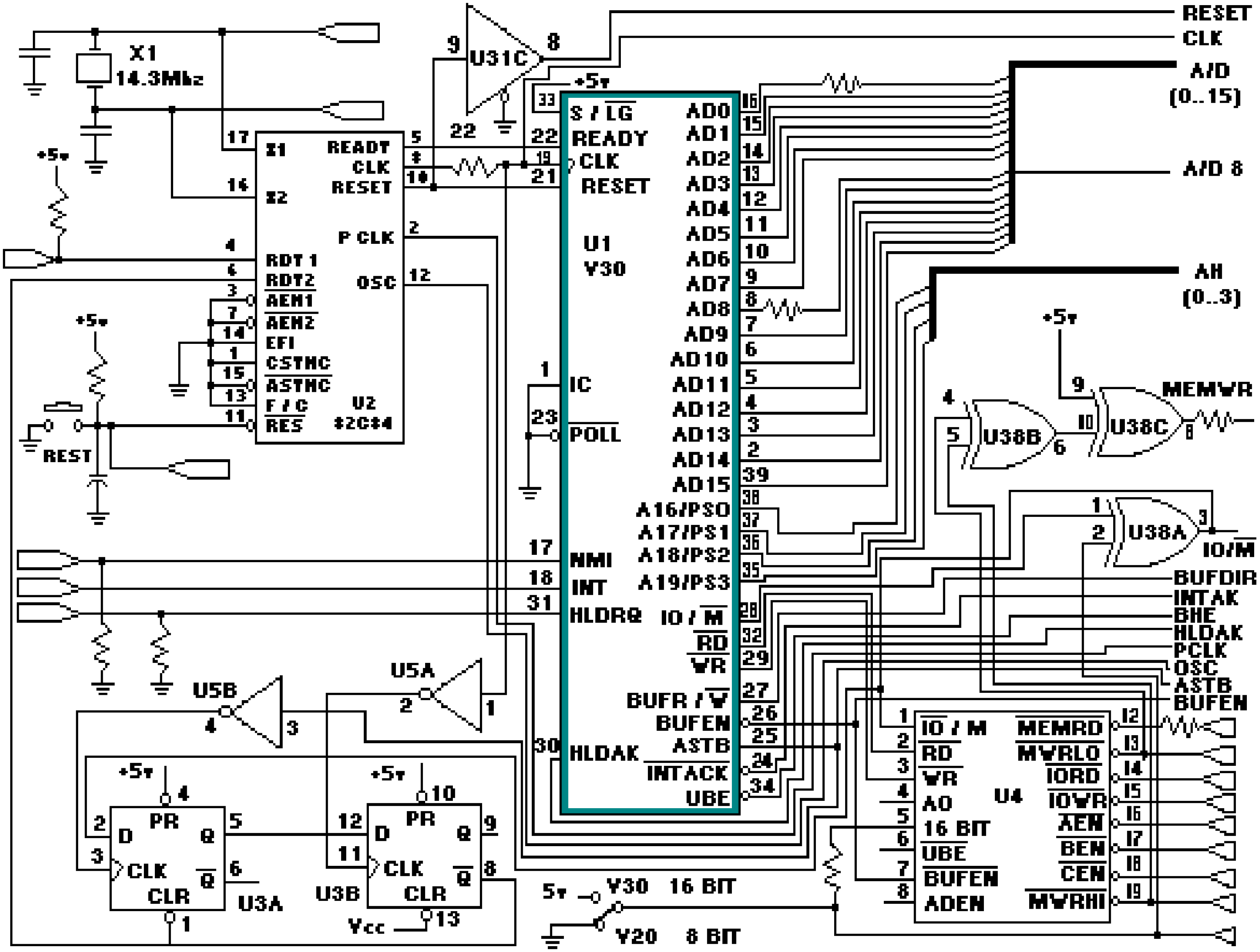
THE U2 CLOCK GENERATOR

Provides the Clock, Ready, and Reset signals for the U1 CPU.

The crystal oscillator provides the raw clock signal for the entire system. 14.31 MHz.

This frequency is divided by three by the U2 to produce the 4.77 MHz used by the U1.

The Ready and Reset signals are passed through the U2 to synchronize them with the U1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U31C
RESET
CLK
A/D
(0..15)
A/D 8
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(0..3)
U1
V30
U2
82C84
REST
U38B
U38C
MEMWR
U38A
IO/M
BUFDIR
INTAK
BHE
HLDAK
PCLK
OSC
ASTB
BUFEN
U5A
U5B
U3A
U3B
U4
Vcc
Y30 16 BIT
Y20 8 BIT
MEMRD
MWRLO
IORD
IOWR
AEN
BEN
CEN
MWRHI

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Enabling Learning Objective

ACTION: Identify the programmable logic array functions in the NIDA 500 microprocessor.

CONDITIONS: Given a classroom environment, Computer Aided Instruction (CAI) workstation, NIDA electronic trainer, and official OMEMS reference material.

STANDARDS: Correctly answer 7 of 10 questions on the CPU Address and Data Bus operations.

THE U4 DECODER

Mode Controller

Controls the Memory and I/O functions.

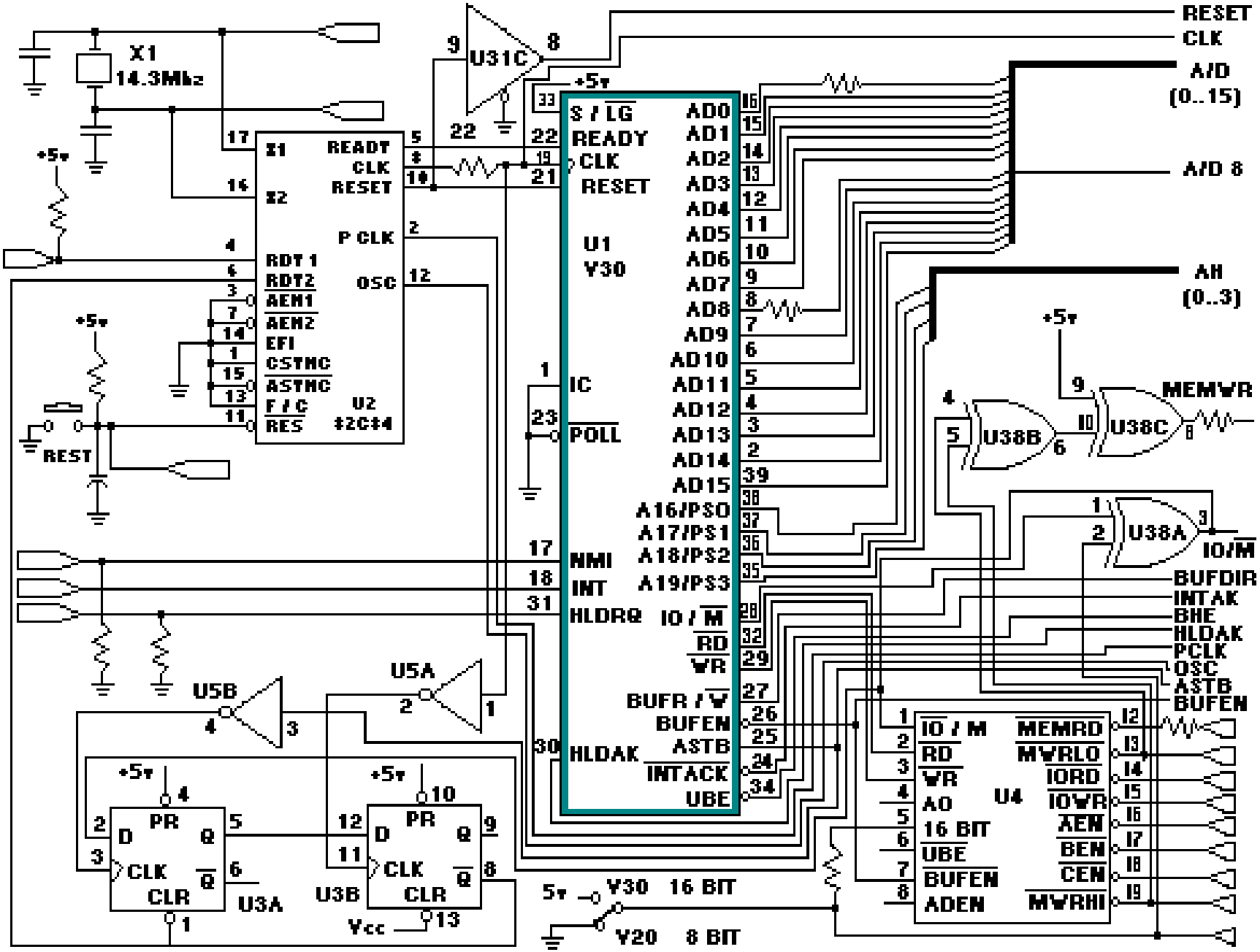
Receives from the U1:

IO/M, RD, WR, UBE, BUFEN, A0

Provides:

$\overline{MEMRD}$, $\overline{MWRLO}$, $\overline{MWRHI}$, $\overline{IOWR}$, $\overline{I/ORD}$, AEN, BEN, CEN (ONLY THE 8 BIT MODE)

USED IN CF351L05-11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RESET
CLK
A/D
(0..15)
A/D 8
AH
(0..3)
+5v
U1
V30
S / LG
READY
CLK
RESET
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
A16/PS0
A17/PS1
A18/PS2
A19/PS3
IO / M
RD
WR
BUFR / R
BUFEN
ASTB
INTACK
UBE
IC
POLL
NMI
INT
HLDRQ
HLDAK
U2
READY
CLK
RESET
P CLK
OSC
RDY1
RDY2
AEN1
AEN2
EFI
CSYNC
ASYNC
F / C
RES
U38B
U38C
MEMWR
U38A
IO/M
BUFDIR
INTAK
BHE
HLDAK
PCLK
OSC
ASTB
BUFEN
U5A
U5B
U3A
U3B
PR
D
CLK
CLR
Q
Vcc
U4
MEMRD
MWRLO
IORD
IOWR
AEN
BEN
CEN
MWRHI
16 BIT
ADEN
V30 16 BIT
V20 8 BIT
REST

CF351L05-

Enabling Learning Objective

ACTION: Identify the operation of the Address Bus.
CONDITIONS: Given a classroom environment, Computer Aided Instruction (CAI) workstation, NIDA electronic trainer, and official OMEMS reference material.
STANDARDS: Correctly answer 7 of 10 questions on the CPU Address and Data Bus operations.

ADDRESS BUS

-20 Address Pins **AD0-AD19**

-Unidirectional – only carries information out from the processor.

-Part of the common bus shared by the data bus.

-Connected to system components that require address information.

LATCHES

-Demultiplexes the address information off of the common bus.

-Retains the address to “point” to a specific location in memory.

LATCHES

3 OUTPUT STATES

	AEN	ASTB
TRANSPARENT	Active	Active
LATCHED	Active	Inactive
HIGH IMPEDANCE	Inactive	Inactive

CONTROL SIGNALS

$\overline{\text{MEMRD}}$, $\overline{\text{MWRLO}}$, $\overline{\text{MWRHI}}$, $\overline{\text{I/OWR}}$, $\overline{\text{I/ORD}}$

These control signals are used in conjunction with the ASTB and the AEN to use the memory or I/O ports.

Before the control signals can be used the address information must be stable in the address latches.

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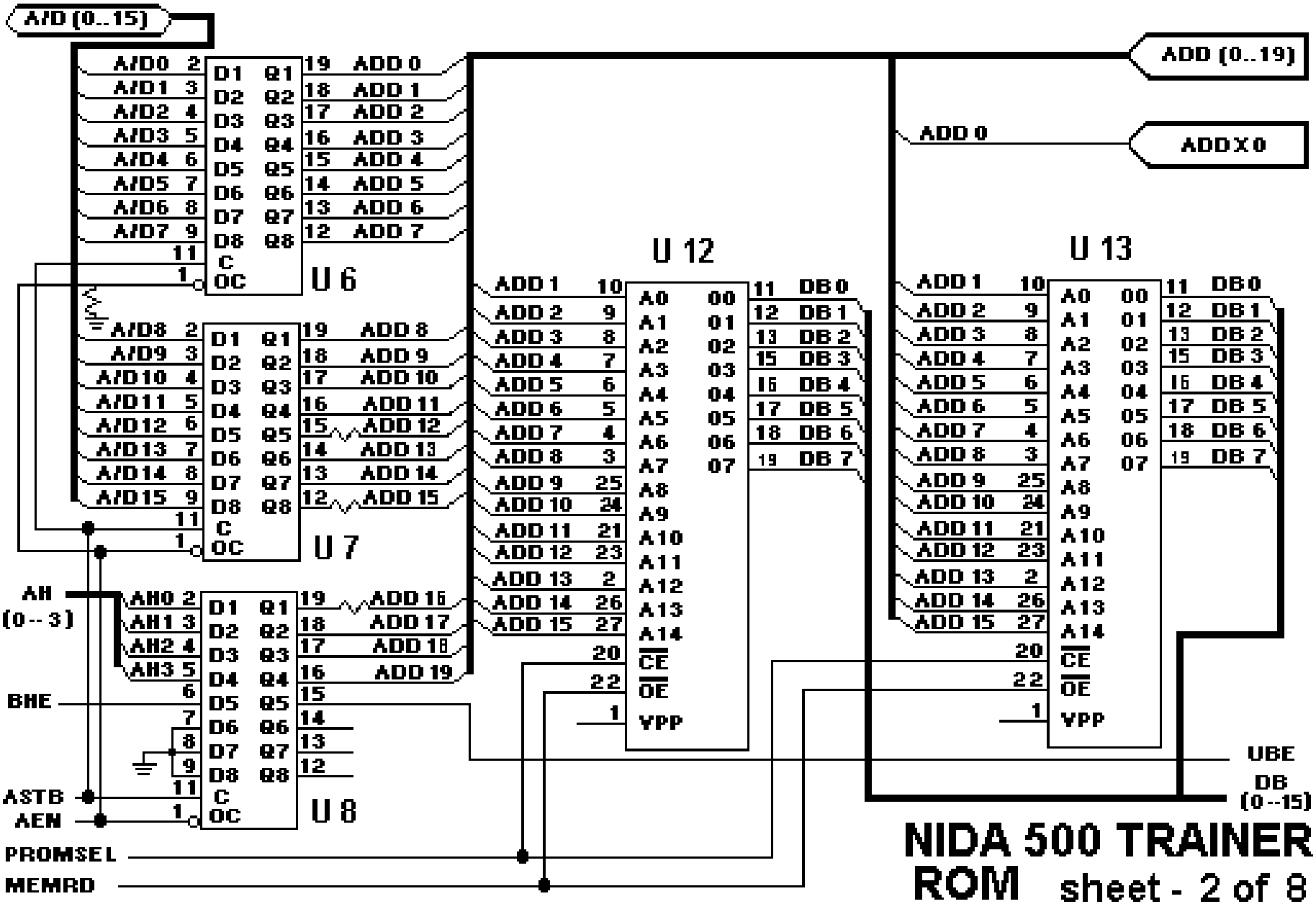
A/D (0..15)
A/D0 2
A/D1 3
A/D2 4
A/D3 5
A/D4 6
A/D5 7
A/D6 8
A/D7 9
11
1
D1 Q1
D2 Q2
D3 Q3
D4 Q4
D5 Q5
D6 Q6
D7 Q7
D8 Q8
C
OC
19 ADD 0
18 ADD 1
17 ADD 2
16 ADD 3
15 ADD 4
14 ADD 5
13 ADD 6
12 ADD 7
U 6
A/D8 2
A/D9 3
A/D10 4
A/D11 5
A/D12 6
A/D13 7
A/D14 8
A/D15 9
11
1
19 ADD 8
18 ADD 9
17 ADD 10
16 ADD 11
15 ADD 12
14 ADD 13
13 ADD 14
12 ADD 15
U 7
AH
(0 -- 3)
AH0 2
AH1 3
AH2 4
AH3 5
6
7
8
9
11
1
19 ADD 16
18 ADD 17
17 ADD 18
16 ADD 19
15
14
13
12
U 8
BHE
ASTB
AEN
PROMSEL
MEMRD
ADD 1 10
ADD 2 9
ADD 3 8
ADD 4 7
ADD 5 6
ADD 6 5
ADD 7 4
ADD 8 3
ADD 9 25
ADD 10 24
ADD 11 21
ADD 12 23
ADD 13 2
ADD 14 26
ADD 15 27
20
22
1
A0 00
A1 01
A2 02
A3 03
A4 04
A5 05
A6 06
A7 07
A8
A9
A10
A11
A12
A13
A14
CE
OE
VPP
11 DB 0
12 DB 1
13 DB 2
15 DB 3
16 DB 4
17 DB 5
18 DB 6
19 DB 7
U 12
U 13
ADD (0..19)
ADD 0
ADDX 0
UBE
DB
(0 -- 15)
NIDA 500 TRAINER
ROM sheet - 2 of 8

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Enabling Learning Objective

ACTION: Identify the operation of the Data Bus.

CONDITIONS: Given a classroom environment, Computer Aided Instruction (CAI) workstation, NIDA electronic trainer, and official OMEMS reference material.

STANDARDS: Correctly answer 7 of 10 questions on the CPU Address and Data Bus operations.

DATA BUS

-Connected to the CPU, Data Buffers, and the Output Latches.

-16-bits wide and bi-directional.

-The buffers allow the data to pass to the memory or CPU when the proper control signals are given. AEN, BEN, BUFDIR

BUS TRANSCEIVERS

Data Buffers

-U9, U10, U11

-The V30 uses buffers U9 and U11. The V20 uses U9 and U10.

-They provide a synchronous two-way communications link between the CPU and other system components.

-Allows the transmission of data only when the control signals are sent to prevent the data being corrupted with

BUS TRANSCEIVER CONTROL SIGNALS

The signals that control the buffers are the:

-DIR which selects the direction of the data flow.

-G Input which enables or disables the buffers.

-The BUFR/W is connected to the DIR pin on the buffers

CONTROL SIGNALS FOR DATA TRANSFER INSTRUCTIONS

IO/$\overline{M}$, $\overline{RD}$, $\overline{WR}$, A0, $\overline{UBE}$, $\overline{BUFEN}$

These signals are generated by the CPU and sent to the U4 decoder.

MODE CONTROLLER GENERATED SIGNALS

$\overline{\text{MEMRD}}$, $\overline{\text{MWRLO}}$, $\overline{\text{MWRHI}}$, $\overline{\text{IORD}}$, $\overline{\text{IOWR}}$

AEN, BEN, CEN

These signals are generated by the U4 decoder in order to control the memory and I/O functions.

The CEN is only used in the V20 8088 mode.

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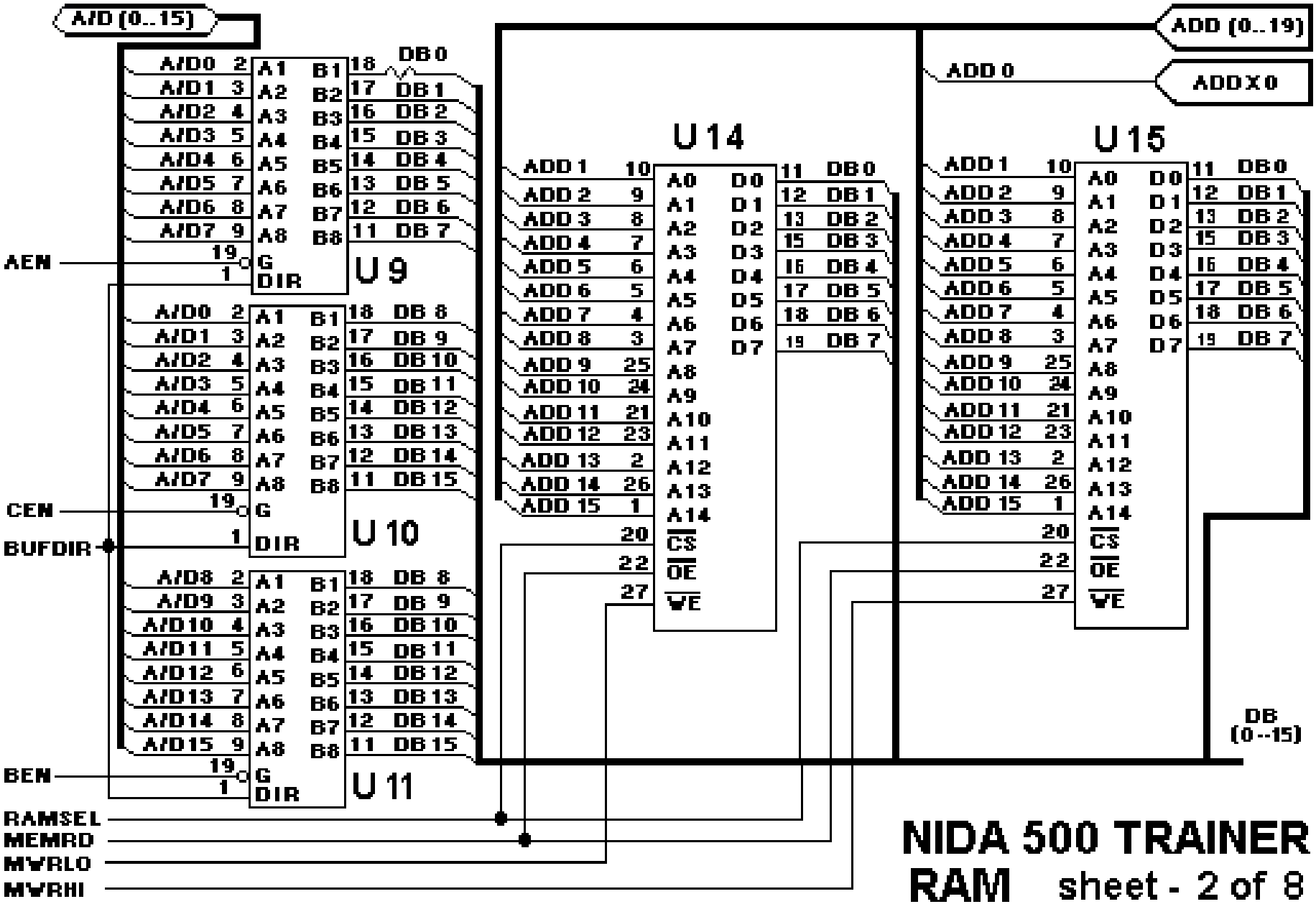
A/D (0..15)
ADD (0..19)
ADD 0
ADDX 0
DB 0
U 9
U 10
U 11
U 14
U 15
AEN
CEN
BUFDIR
BEN
RAMSEL
MEMRD
MWRLO
MWRHI
DB (0--15)
NIDA 500 TRAINER
RAM sheet - 2 of 8
CF351L05-

Review

The V30 is similar to what type of processor?

A. 8080

B. 8086

C. 8088

D. Pentium 4 1.7 GHz

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B. 8086

C. 8088

D. Pentium 4 1.7 GHz

Review

Why are the Ready and Reset signals sent through the U2?

A. To make sure they are the correct levels for the processor.

B. To send them to the decoder.

C. To synchronize them to the clock signal.

D. To change them to the opposite state.

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Review

What signal is not sent to the decoder from the U1?

A. $\overline{\text{UBE}}$.

B. IO/$\overline{\text{M}}$.

C. $\overline{\text{WR}}$

D. 16 BIT.

Review

What signal is not sent to the decoder from the U1?

A. $\overline{\text{UBE}}$

B. $\text{IO}/\overline{\text{M}}$

C. $\overline{\text{WR}}$

D. $\underline{\text{16 BIT}}$

Review

What two buffer chips are used with the V30?

A. U9, U11

B. U9, U10

C. U6, U7

D. U6, U8

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